AMENDMENTS TO THE SPECIFICATION:

Please insert the following caption on page 6, between lines 4 and 5:

SUMMARY

Please amend paragraph [0010] on page 6, as follows:

[0010] An object of the ~~present invention~~ technology disclosed herein is to provide a semiconductor device which has such high reliability that the forward voltage difference ΔVf representing forward voltage deterioration is not more than 1.0 V as well as a manufacturing method therefor.

Please amend paragraphs [0012] through paragraph [0016] beginning on page 6 and continuing through page 8, as follows:

[0012] According to the ~~present invention~~ technology disclosed herein, since the first- and second-conductive-type silicon carbide semiconductor layers are formed as described above, semiconductor layers less liable to basal plane dislocation can be obtained. As a result, a pn junction diode which is less liable to forward voltage deterioration and long in service life can be obtained.

[0013] In one example embodiment ~~of the invention~~ the bipolar semiconductor device further includes

at least one layer of a first- or second-conductive-type silicon carbide semiconductor formed on the drift layer.

[0014] According to the example embodiment, since the first- and second-conductive-type silicon carbide semiconductor layers are formed as described above, semiconductor layers less liable to basal plane dislocation can be obtained. As a result, a pn junction diode or a bipolar transistor which is less liable to forward voltage deterioration and long in service life can be obtained.

[0015] In one example embodiment ~~of the invention~~,

the substrate serves as a cathode and

the bipolar semiconductor device further includes a semiconductor layer which is formed on the drift layer and which is of a second-conductive-type silicon carbide to serve as an anode.

[0016] According to the example embodiment, since the first- and second-conductive-type silicon carbide semiconductor layers are formed as described above, semiconductor layers less liable to basal plane dislocation can be obtained. As a result, a pn junction diode which is less liable to forward voltage deterioration and long in service life can be obtained.

Please amend paragraph [0024] on page 11, as follows:

[0024] According to the ~~present invention~~ technology disclosed herein, since the propagation of the basal plane dislocation in the semiconductor layers is suppressed, forward voltage deterioration can be prevented. That is, the forward voltage difference ΔVf representing forward voltage deterioration can be suppressed to 1.0 V or less, so that a high-reliability bipolar device can be made up. With the use of such a high-reliability bipolar device, power conversion equipment, such as inverters, which are reduced in loss, capable of long-term operation and high in reliability can be implemented.

Please amend paragraphs [0025] through [0031] on page 12, as follows:

[0025] Fig. 1 is a sectional view of a pn (pin) diode which is a First Example Embodiment ~~of the present invention~~;

[0026] Fig. 2 is a graph showing current-voltage characteristics of the pin diode of the First Example Embodiment ~~of the invention~~ at a start of energizing and one hour after the energizing;

[0027] Fig. 3 is a graph showing current-voltage characteristics of a pin diode of the First Example Embodiment ~~of the invention~~ and a pin diode using a Si surface substrate made for comparison before deterioration, i.e. immediately after the conduction, and after deterioration, i.e. after the one-hour conduction;

[0028] Fig. 4 is a sectional view of an npn bipolar transistor ~~which is~~of a Second Example Embodiment~~of the invention~~;

[0029] Fig. 5 is a sectional view of an IGBT ~~which is~~for a Third Example Embodiment ~~of the invention~~ is formed;

[0030] Fig. 6 is a perspective view showing a crystal of silicon carbide ~~from which~~for a substrate of the bipolar semiconductor device ~~of the invention~~;

[0031] Fig. 7 is a perspective view showing a crystal of silicon carbide ~~from which~~for a substrate of a conventional bipolar semiconductor device ~~is formed~~.

Please amend the heading on page 14, line 12, as follows:

~~BEST MODE FOR CARRYING OUT THE INVENTION~~DETAILED DESCRIPTION

Please amend paragraph [0033] on page 14, as follows:

[0033] Hereinbelow, an example embodiment ~~of the invention~~ will be described in detail. In the description of crystal lattice orientations and lattice surfaces, the following symbols, which are well known in the related technical fields, are used to represent lattice orientations and lattice surfaces. That is, an individual surface is expressed by (), and a set surface is by {}, where respective numerals are enclosed therein to represent individual surfaces. Also, whereas the negative index is represented by adding a "-" (bar) on a numeral in crystallography, it is impossible to added a bar above a numeral by software designated by JPO (Japanese Patent Office) and therefore a negative sign is added before a numeral for expression in this specification.

Please amend paragraphs [0039] and [0040] on page 16, as follows:

[0039] Which growth goes, the step flow or the two-dimensional nucleation, depends largely on the supersaturation in crystal surfaces. When the supersaturation goes beyond a certain value (critical supersaturation), the two-dimensional nucleation growth goes. With the supersaturation under the certain value, the step flow growth goes. Therefore, given a large critical supersaturation, the two-dimensional nucleation is less likely to occur.

[0040] ~~For obtainment of~~To obtain a large critical supersaturation, the growth rate is increased by, for example, increasing the feed amount of material gas, or by reducing the off-angle of the crystal to widen the terrace (flat portions) of a step present in crystal surfaces.

Please amend paragraphs [0044] through [0046] beginning on page 18, as follows:

[0044] In ~~the~~an example embodiment ~~of the present invention~~, semiconductor layers including an n-type layer, a p-type layer and the like constituting the SiC bipolar semiconductor device are formed on a surface 2a having a specified off-angle θ relative to the (000-1) carbon surface 2 of the SiC crystal. The off-angle θ is determined for an optimum angle within a range of 2 to 10 degrees depending on the type of the semiconductor device. According to an experiment by the inventors, successful results were obtained with an off-angle θ of about 8 degrees in the case of, for example, a pin diode. For an IGBT, successful results were obtained with an off-angle θ of about 3.5 degrees. Furthermore, the growth rate of the semiconductor layers is set faster than ordinary ones. The growth rate is desirably so set that the thin-film increasing amount per hour (h) becomes 10 μm/h or more. Depending on film growth conditions, the effect of the ~~invention~~technology disclosed herein can be obtained even with film growth rates of 3 μm/h or more. In order to increase the growth rate, the amount of material gas to be fed during the film growth process is increased to a large extent.

[0045] Hereinbelow, preferred example embodiments ~~of the present invention~~ are explained with reference to Figs. 1 to 6.

[0046] (First Embodiment)

Fig. 1 is a sectional view of a pn (pin) junction diode which is a First Example Embodiment of a bipolar semiconductor device ~~of the present invention~~. In this Embodiment, semiconductor layers to be described below are formed on an n-type (first conductive type) 4H SiC substrate 21 whose surface orientation has an off-angle of 8 degrees from the (000-1) carbon surface. In the term "4H," the character "H" means hexagonal crystal and the numeral "4" means a crystal structure whose atomic lamination is four-layer cyclic. The C surface of the substrate 21 is a surface 2a having an off-angle θ of 8 degrees from the (000-1) carbon surface 2 of SiC crystal of Fig. 6. The film growth rate for each layer is 15 μm/h, where the increasing rate of film thickness per hour (h) is faster than in the conventional counterpart. Then, as described in detail below, n-type (first conductive type) 4H-SiC layer and p-type (second conductive type) 4H-SiC layer are epitaxially grown one by one, by which an epitaxial pin junction diode 70 is fabricated. A primary junction surface of the p-type layer and an i layer (insulating layer), and a primary junction surface (a surface extending in the horizontal direction in Fig. 1) of the i layer and the n-type layer, are both a {0001} surface.

Please amend paragraphs [0070] and [0071] beginning on page 28, as follows:

[0070] As described above, the pin junction diode of SiC of this Embodiment, because of its being almost free from occurrence of forward voltage deterioration, becomes capable of long-term use, e.g., long ~~in serve~~service life. Since the pin junction diode is free from increases in on-resistance due to forward voltage deterioration, a high-reliability pin junction diode which is free also from internal loss and which is capable of maintaining stable characteristics for long time can be obtained.

[0071] (Second Embodiment)

Fig. 4 is a sectional view of an npn bipolar transistor 50 which is a Second Example Embodiment of ~~the~~ a bipolar semiconductor device ~~of the invention~~. In this embodiment also, as shown in Fig. 6, an n-type 4H SiC substrate having a surface 2a whose surface orientation has an off-angle θ of 8 degrees from the (000-1) carbon surface 2 (hereinafter, referred to as C surface) is used. On this substrate, n-type 4H-SiC, p-type 4H-SiC and n-type 4H-SiC are successively epitaxially grown in this order with a film-thickness increasing rate per hour (h) of 15 μm/h, by which an npn bipolar transistor 50 was fabricated.

Please amend paragraph [0094] on page 36, as follows:

[0094] (Third Embodiment)

A Third Example Embodiment relates to an IGBT (Insulated Gate Bipolar Transistor) which is a bipolar semiconductor device ~~of the present invention~~. Fig. 5 is a sectional view of an IGBT 60 of this Embodiment. In this Embodiment, a substrate 61 (hereinafter, referred to as C surface substrate) using n-type 6H SiC whose surface orientation has an off-angle θ of 3.5 degrees from the (000-1) carbon surface 2 in Fig. 6 is prepared. On the substrate 61, three layers, i.e. a p-type 6H-SiC layer, an n-type 6H-SiC layer and a p-type 6H-SiC layer, are epitaxially grown in this order with a film-thickness increasing rate per hour (h) of 15 μm/h, by which an IGBT 60 is fabricated as is explained in detail below. The primary junction surface (a surface extending horizontally in the figure) of the p and n layers is the {0001} surface.

Please amend paragraph [0115] on page 42, as follows:

[0115] As described above, ~~the~~three example embodiments of bipolar semiconductor device ~~of the present invention has~~have been described ~~based on three Embodiments~~. However, the invention is not limited to the above Embodiments, but is applicable also to various kinds of 4H-SiC bipolar semiconductor devices such as SIAFETs, SIJFETs, thyristors, GTOs, MCTs (Mos Controlled Thyristors), SiCGT (SiC Commutated

Gate Thyristors), ESTs (Emitter Switched Thyristors), and BRTs (Base Resistance Controlled Thyristors). Naturally, the invention can be modified and applied to various kinds of 4H-SiC bipolar devices such as opposite-polarity devices (e.g., pnp transistors for npn transistors), and further applicable to SiC bipolar devices using 6H-SiC or other crystal structures.